DEVELOPMENT OF MICROSYSTEMS WITH ZEOLITE LAYERS: MASS SENSORS & MICRO-REACTORS

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Zeolites are nano-structured materials like hydrated aluminous-silicates with several applications. One of the most important advantages of these materials is the crystalline and well defined structure. Zeolites porous are the same size of the most common molecules, between 0.3 and 1.1 nm. Therefore the nano-scale interactions between wall porous and adsorbed molecules are strong. The size and shape of these channels, their large surface area, as well as their variable hydrophilic/hidrophobicity make these materials ideal candidates as specific adsorbents of organic molecules or water in the gas phase.

In addition to the classical applications in sorption and catalysis, zeolites are attractive for novel technologies including highly selective separation membranes, host-guest systems, and chemical sensors. During the last years, a great development of the application of zeolites and related materials like new materials in the field of nanotechnology has been experienced [1].

The aim of this work is the preparation of thin zeolite films on silicon wafer and the design of micro-structures using technologies based on silicon. Of this way, we want to obtain a free standing zeolite microcantilever, supported micromembranes and microreactors.

A good and continuous zeolite layer has been grown up or deposited on 3" silicon wafers, in this case zeolite synthesized is SIL-1 (figure 1). Using lithography techniques, different designs have been prepared on resin, and after, these structures have been made via chemical and physical etchings. Via chemical have been run with different acid like HF and H₃PO₄ and basic like KOH and TMAH (tri-methyl-ammonium hydroxide), it depends of the material to be etched. Via physical, we have used RIE (Reactive Ion Etching) and Ion milling, both available ones in our laboratories. Same results are showed in the figures 2 and 3.

In conclusion, we can say that it is possible to build microstructures in zeolite layers on silicon wafers. These results are a good start to establishing the suitable conditions for futures MEMS developments.

References:

[1] Corma A. and Garcia H. Europ. J. Inorg. Chem. 6 (2004), 1143-1164.

Figurer:

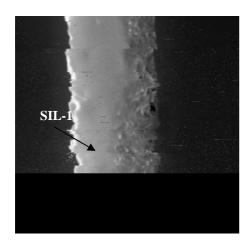


Figure 1: transversal section of SIL-1 layer on silicon wafer.

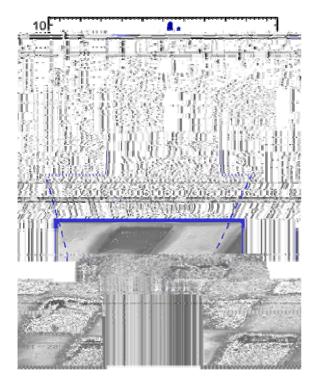


Figure 3: HF etching in SIL-1 layer on silicon wafer

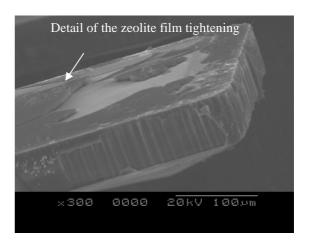


Figure 2: SIL-1 layer deposited on cantilever by chemical linkage.

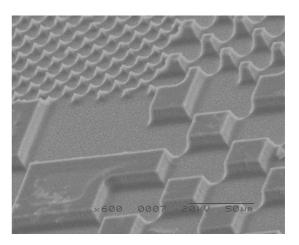


Figure 4: RIE etching in SIL-1 layer on silicon wafer.